



Fig. 1  
(PRIOR ART)



```
`celldefine
`ifdef verifault
    `suppress_faults
    `enable_portfaults
`endif
module ROM ( ... );
output ...; input ...; wire ...;
reg [3:0] _doutr;
reg [3:0] rom_data [0:127];
    //control circuit
    buf ( _H15,H15 );
    ....
    //data out
    buf ( N01,_dout[0] );
    ....
    //address
    buf ( _H07,H07 );
    buf ( _H14,H14 );
    and ( _a[6],_H07,_H15 );
    and ( _ta[6],_H14,_TEB );
    or ( _ad[6],_a[6],_ta[6] );
initial
    $readmemh("file",rom_data );
always @ _ad // read port
    if ( _ad <= 127 )
        _doutr = rom_data[_ad];
    else
        _doutr = 4'bx;
specify
...
endspecify
endmodule
`ifdef verifault
    `nosuppress_faults
    `disable_portfaults
`endif
`endcelldefine
```

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**FIG.5**  
(Conventional Art)